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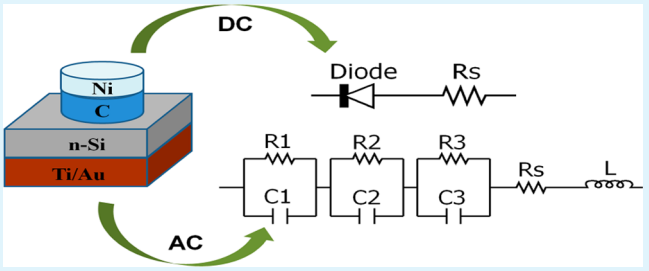
Investigation of the Interfaces in Schottky Diodes Using Equivalent Circuit Models

Chanyoung Yim,[†,‡] Niall McEvoy,[‡] Hye-Young Kim,[‡] Ehsan Rezvani,[†,‡] and Georg S. Duesberg*[,†,‡]

[†]School of Chemistry and [‡]Centre for Research on Adaptive Nanostructures and Nanodevices (CRANN), Trinity College Dublin, Dublin, 2, Ireland

Supporting Information

ABSTRACT: The metal–semiconductor contact is one of the most critical factors that determine the performance of semiconductor devices such as Schottky barrier diodes (SBDs). SBDs between conductive carbon thin films and silicon have attracted attention due to their high performance and potential low cost of fabrication. Here, we introduce impedance spectroscopy (IS) as a powerful technique to characterize such SBDs. The electrical and structural characteristics of carbon–silicon SBDs between silicon and two different types of conductive carbon thin films have been investigated. Modeling the data with an extended equivalent circuit model reveals the effects of the metal electrode contacts of SBDs for the first time. From dc current–voltage measurements, diode parameters including the ideality factor, the Schottky barrier height, and the series resistance are extracted. Through use of analysis with IS, additional information on the Schottky contact is obtained, such as the built-in potential and more reliable barrier height values. Thus, IS can be utilized to analyze interfaces between metals and semiconductors in great detail by electrical means.



KEYWORDS: *metal–semiconductor contact, Schottky diode, conductive carbon thin films, interface analysis, equivalent circuit model, impedance spectroscopy*

1. INTRODUCTION

Metal–semiconductor (M-S) contacts occur in numerous electronic devices, and as diodes they are used for power and frequency control circuits. It is well-known that the quality of M-S contacts is one of the most critical factors which determine the performance of semiconductor devices or integrated circuits. When a metal makes contact with a semiconductor, an energy barrier is formed at the interface. This barrier controls the current conduction at the interface. M-S contacts show either rectifying or ohmic behavior at the contact area depending on the difference in work function of the two materials. Ohmic contacts are important in high performance semiconductor devices, while rectifying contacts (i.e.,Schottky contacts) are essential for various electronic devices. In particular, Schottky contacts can be utilized to test the physical and electrical properties of a semiconductor material and its surfaces.[1,2] For example, a Schottky diode was adopted to characterize bulk defects and investigate interface effects of M-S systems.[3−5] Therefore, comprehension of the fundamental physical and electrical properties of M-S systems is of great importance for assisting the development of technologies aimed at forming high quality M-S contacts, crucial for various device applications.

To define the electrical characteristics of M-S contacts, dc current–voltage (J–V) and capacitance–voltage measurement techniques have typically been employed. Impedance spectroscopy (IS) is a powerful method for characterizing the electrical properties of materials and their interfaces, and it can be used to investigate the dynamics of bound or mobile charge in the bulk or interfacial regions of any kind of solid or liquid material.[6] In recent years, IS has been applied to investigate the electrical characteristics and conduction mechanism of various organic and inorganic semiconductor devices such as organic light-emitting diodes (OLEDs), organic thin film transistors (OTFTs), and solar cells.[7−13] In particular, the interfacial region of M-S contacts can be characterized with an appropriate equivalent circuit model developed from the impedance spectra. Although some analytical approaches have been introduced to describe the conduction mechanism between a metal electrode and a single individual semiconducting nanowire,[14,15] analyses of the electrical nature of the Schottky contacts in diode devices using ac impedance measurements have rarely been reported.

In this paper, we investigate carbon–silicon interfaces in Schottky barrier diode (SBD) devices. The devices were fabricated with two different conductive carbon thin films as metallic layers on silicon substrates. Conductive carbon materials such as glassy or pyrolytic carbon have been investigated due to their high electrical conductivity, durability, and low cost.[16,17] In particular, pyrolytic carbon, a disordered

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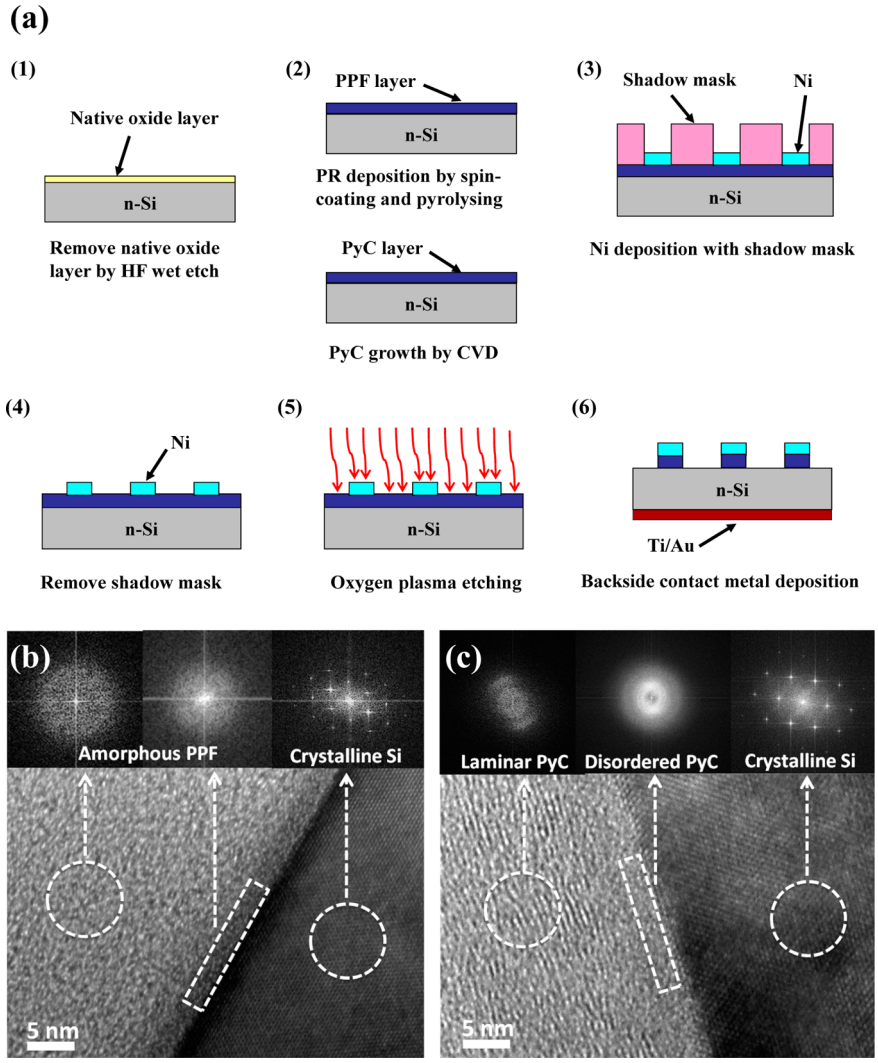

Figure 1. (a) Process flow of the carbon–silicon SBD fabrication. Cross-sectional HRTEM images (bottom) and selected area diffraction patterns (top) of (b) the PPF/n-Si interface and (c) the PyC/n-Si interface.

nanocrystalline graphitic material, has been suggested for electronic device applications including vias/wires, gate electrodes, and Schottky diode devices.[18−21] We used both dc $J-V$ and ac IS analysis methods to investigate the electrical characteristics of the carbon–silicon SBDs alongside structural characterization. From the dc $J-V$ measurement, diode parameters of the conventional equivalent circuit model including the ideality factor, n, the barrier height, φ_B, and the series resistance, R_S, are determined. From the ac impedance measurements, under various dc bias conditions, an advanced equivalent circuit model which offers more insight into the system was developed. As a result, a deeper understanding of the electrical properties of M-S contacts is possible using the introduced methods.

2. EXPERIMENTAL DETAILS

Device Preparation. The devices were fabricated on n-type silicon (n-Si) wafers with a dopant (phosphorus) concentration of 5×10^{14} cm^{-3} and ⟨100⟩ orientation. Two different types of conductive carbon thin films were deposited as electrodes. Pyrolyzed photoresist films (PPF) were produced by pyrolysis of thin films of AZ nLOF 2070, a negative tone photoresist. This was performed at 1000 °C in a forming gas atmosphere as described in detail previously.[16] Thin films of pyrolytic carbon (PyC) were grown by chemical vapor deposition (CVD). This process entailed the decomposition of an acetylene (C_2H_2) precursor at a temperature of 950 °C. A growth time of 5 min was employed to give a film thickness of ∼60 nm, as described previously.[17]

Diodes were fabricated from these carbon films using a process described in detail elsewhere;[21] a process flow of this is presented in Figure 1a. Briefly, this entailed depositing arrays of Ni dots (50 nm thick) onto the films, using a shadow mask to define the active device area. Oxygen plasma etching was used to remove the carbon film in regions not protected by Ni dots, thus producing an array of isolated carbon–silicon Schottky barrier diodes. Ohmic contacts were made on the backside of the Si substrate by depositing Ti (20 nm) and Au (40 nm). A Gatan model 682 PECS was used for the deposition of all metal layers.

Characterization. The diodes were characterized as previously described.[21] Cross sections of the interface of both PPF and PyC with Si were prepared using a Zeiss Auriga Dual Beam focused ion beam (FIB). High resolution transmission electron microscopy (HRTEM) studies of these cross sections were performed using an FEI Titan 80-300 (S) transmission electron microscope operated at 300 kV. A Suss probe station, connected to a Keithley 2612 A source meter unit, was used for dc electrical measurements. IS measurements were carried out using a Gamry Reference 600 potentiostat with a two-electrode mode configuration and GamryEchem Analyst software was used for the data analysis.

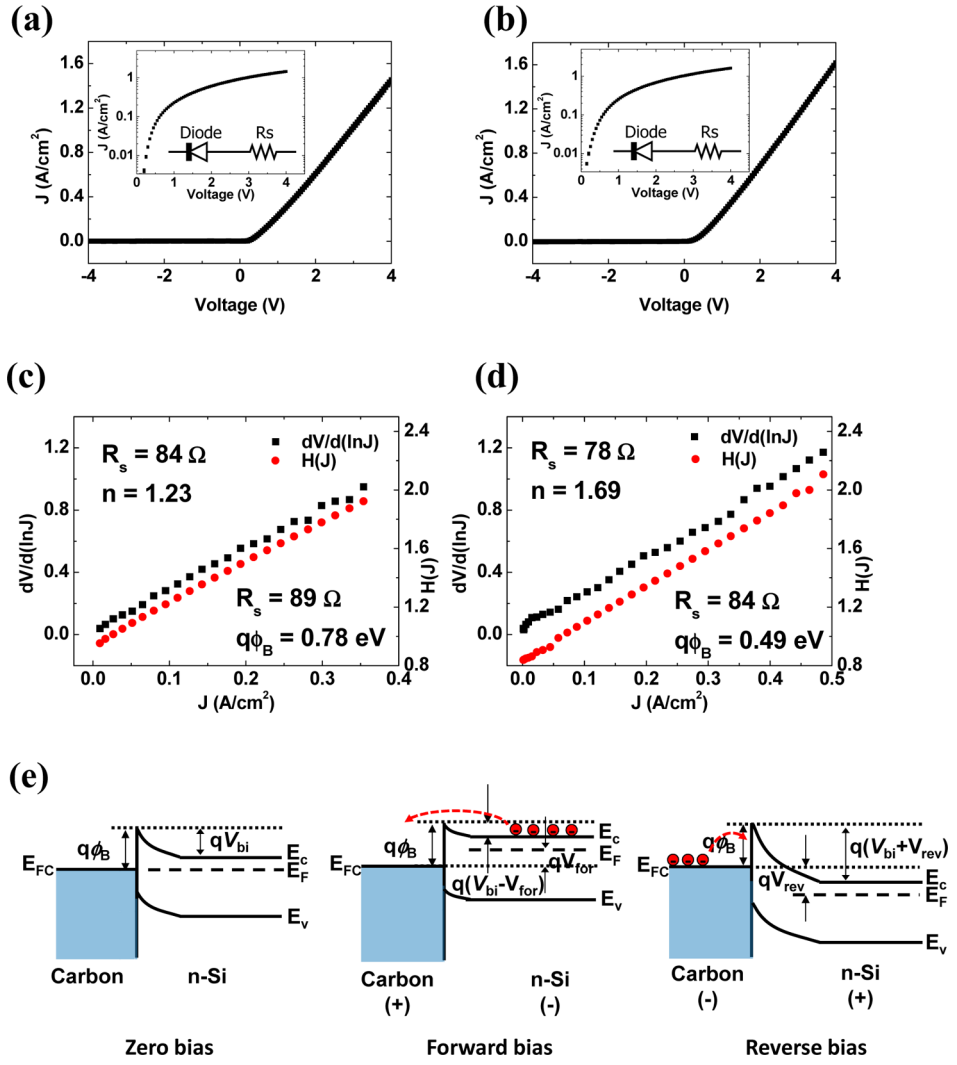

Figure 2. $J-V$ measurements of (a) the PPF/n-Si SBD and (b) the PyC/n-Si SBD on a linear scale. Insets denote the plots on a semilogarithmic scale and the dc equivalent circuit model of the diode. Plots of $dV/d(\ln J)$ vs J and $H(J)$ vs J for (c) the PPF/n-Si and (d) the PyC/n-Si SBDs. (e) Energy-band diagram of a conductive carbon thin film on n-Si substrates under zero, forward and reverse bias. φ_B, E_c, E_v, E_F, E_{FC}, V_{bi}, V_{for}, and V_{rev} indicate the Schottky barrier height, bottom energy of conduction band of n-Si, top edge of valence band of n-Si, Fermi energy level of n-Si, Fermi energy level of carbon, built-in potential, forward bias, and reverse bias, respectively.

3. RESULTS AND DISCUSSION

Cross-sectional HRTEM analysis of the interface between carbon thin films and silicon substrates is depicted in Figure 1b and c. The interface region between the bulk PPF and silicon is slightly darker than the bulk PPF region. However, it is obvious from the corresponding diffraction patterns that both the bulk and interface area of the PPF have the same amorphous structure typical for glassy carbon. The PyC layer has a slightly laminar structure parallel to the underlying substrate with a very thin disordered carbon region at the interface, which is clearly verified by the corresponding diffraction patterns.[22] It is believed that a direct link is formed between the crystalline Si and the carbon as there is no interfacial layer (e.g., SiO_2) visible at the contact; however, its existence cannot be completely ruled out by HRTEM analysis. The resistivity values, from four-point measurements on insulating substrates, are 4.0×10^{-5} Ωm for the PPF layer[16] and 2.5×10^{-5} Ωm for the PyC layer.[17] The thickness of the carbon layers was obtained from cross-sectional TEM images[21] and found to be 78−80 nm for the PPF layer and 62−65 nm for the PyC layer.

Figure 2a and b shows the current−voltage ($J-V$) characteristics of PPF/n-Si and PyC/n-Si SBD devices, respectively. The measurements were carried out with a dc bias range of ±4 V under ambient conditions. The Ni metal dot electrodes are positively biased in the forward-bias region, and conversely biased in the reverse-bias region. As reported in our previous work,[21] both devices present clear rectifying behavior, indicating the formation of Schottky contacts between carbon thin films and n-Si substrates. Since the current transport in Schottky contacts can be explained by thermionic emission theory, the relationship between the current density, J, and the voltage drop across the junction, V_D, can be given by the following equation:[2,23]

$$J = J_S\left(\exp\frac{qV_D}{nk_BT} - 1\right) \quad (1)$$

where J_S is the reverse saturation current density and can be expressed as

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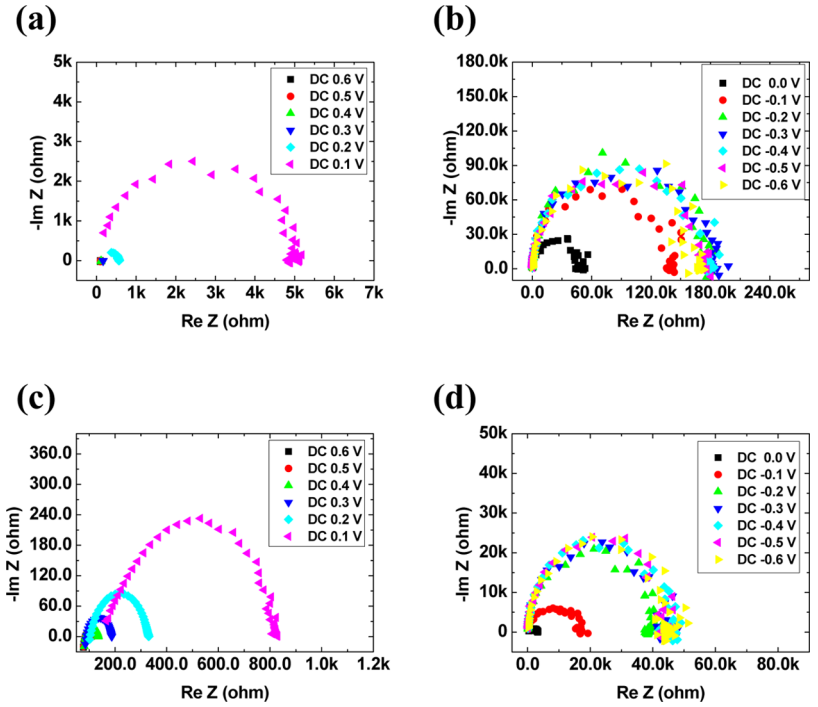

Figure 3. Cole–Cole plots of the PPF/n-Si SBD (a) under forward dc bias voltages and (b) under zero and reverse dc bias voltages. Cole–Cole plots of the PyC/n-Si SBD (c) under forward dc bias voltages and (d) under zero and reverse dc bias voltage with frequencies increasing from the right to the left of the *x* axis (from 1 Hz to 1 MHz).

$$J_S = A^{**}T^2 \exp\left(\frac{-q\phi_B}{k_B T}\right) \tag{2}$$

where q is the elementary charge, T is the absolute temperature, k_B is the Boltzmann constant, n is the ideality factor, A^{**} is the effective Richardson constant which is equal to 112 A cm^{-2} K^{-2} for n-Si, and φ_B is the effective barrier height at zero bias. When the effect of series resistance, R_S, of the system is taken into account, the voltage across the diode can be expressed in terms of the total voltage drop, V, across the series combination of the diode and the resistor. Thus, $V_D = V - JR_S$, and for $V_D > 3k_BT/q$, eq 1 becomes

$$J = J_S \exp\left[\frac{q(V - JR_S)}{nk_BT}\right] \tag{3}$$

Therefore, the carbon–silicon SBDs can be modeled with a conventional equivalent circuit model with the ideality factor n and the series resistance R_S as shown in the inset of Figure 2a and b. Using Cheung's method,[24] eq 3 can be rewritten:

$$V = JAR_S + n\phi_B + \left(\frac{nk_BT}{q}\right)\ln\left(\frac{J}{A^{**}T^2}\right) \tag{4}$$

where A is the effective diode area.

When the eq 4 is differentiated with respect to the current density J, we obtain

$$\frac{d(V)}{d(\ln J)} = JAR_S + \frac{nk_BT}{q} \tag{5}$$

In eq 5, a linear relationship can be expected from the plot of $d(V)/d(\ln J)$ vs J, giving the AR_S value from the slope and the n value from the y-axis intercept of the plot. Also, from eq 4, the auxiliary equation $H(J)$ can be defined as

$$H(J) = V - \left(\frac{nk_BT}{q}\right)\ln\left(\frac{J}{A^{**}T^2}\right) \tag{6}$$

$$H(J) = JAR_S + n\phi_B \tag{7}$$

Using the value of n derived from eq 5 and the result of $H(J)$ from eq 6, the plot of $H(J)$ vs J from eq 7 gives a straight line with y-axis intercept equal to $n\varphi_B$. In addition, the slope of this plot gives the value of series resistance by which the consistency of R_S from eq 5 can be checked. The plots of $dV/d(\ln J)$ vs J and $H(J)$ vs J for the PPF/n-Si and the PyC/n-Si SBD devices are presented in Figure 2c and d. The PPF/n-Si SBD device has R_S values of 84 and 89 Ω derived from the plots of $dV/d(\ln J)$ vs J and $H(J)$ vs J, respectively, which are in good agreement. The values of n and $q\varphi_B$ were found to be 1.23 and 0.78 eV, respectively. In the case of the PyC/n-Si SBD, the values of R_S from the plots of $dV/d(\ln J)$ vs J and $H(J)$ vs J are 78 and 84 Ω, respectively, with the values of n = 1.69 and $q\varphi_B$ = 0.49 eV. A schematic energy-band diagram of the interface between conductive carbon thin films and n-Si substrates under various dc bias conditions is depicted in Figure 2e. A space-charge region accompanied by the built-in potential (V_{bi}) is formed in the n-Si near the carbon/Si interface under zero bias. Depending on the external dc bias, current can flow over the reduced barrier under forward bias, or can be blocked by the Schottky barrier under reverse bias, which is typical rectifying behavior.

Ac impedance spectra of the carbon–silicon SBD devices were recorded in the frequency range of 1 Hz to 1 MHz with an oscillating voltage of 10 mV during dc voltage scanning from −0.6 to +0.6 V in steps of 0.1 V at room temperature. Figure 3 shows the Cole–Cole impedance plots of each carbon–silicon SBD under varying dc bias voltages, in which the implicit variable is the frequency increasing from the right to the left of

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the x axis (from 1 Hz to 1 MHz). It is observed that the impedance spectra are nearly semicircular over the whole dc bias range, implying that the equivalent circuit of the device consists of a combination of resistance and capacitance (RC) networks.[6] The diameter of each semicircular arc corresponds to the total impedance of the device. It should be noted that the several uncompleted semicircles in these plots are due to instrument limitation in this frequency range. In both devices, the radius of the semicircles increases when the positive dc bias is decreased and they further increase under negative bias, outlining the dc bias dependent behavior of RC values of the devices. In addition, some scattering of data are found at low-frequencywhich is more apparent at high reverse bias.

In order to gain a deeper understanding of the Schottky contact, an ac equivalent circuit model was developed. The typical equivalent circuit model of a Schottky diode is composed of a parallel connected RC network and a series resistance which is serially connected to the RC network,[1] as shown in Figure 4a. The capacitance component (C_P) in the equivalent circuit denotes the depletion layer capacitance of the contact, and the parallel resistance component (R_P) is associated with a shunt resistance. However, it is not always possible to match impedance spectra with this simple equivalent circuit since the contact area of each metal electrode can give rise to additional capacitive components in real devices. In this work, the simulated results from the best fit of the typical equivalent circuit model in Figure 4a did not show good fitting with the measured data in the forward dc bias region, although they fitted well in the reverse dc bias region (see Supporting Information Figure S1). Therefore, a more complex version of the equivalent circuit model was developed to interpret the impedance spectra, where the effect of contacts between the carbon and the Ni electrode, and the silicon and the Ti/Au electrode was taken into account. The extended form of the equivalent circuit model of the carbon−silicon SBD structure is presented in Figure 4b. The equivalent circuit model consists of three RC circuits in series lumped with a series resistance R_S and a parasitic inductance L. C_1, C_2, and C_3 are the capacitances associated with a nickel−carbon interface, carbon−silicon interface, and silicon−titanium interface, respectively, with corresponding shunt resistances R_1, R_2, and R_3. The ac impedance of the circuit is given by[6]

$$Z(\omega) = Z'(\omega) - jZ''(\omega) \tag{8}$$

where ω represents the frequency, Z' and Z'' are the magnitudes of the real and imaginary parts of the impedance, respectively, and a negative sign is used for the imaginary part because of the capacitive reactance of the circuit. To mathematically analyze the model in Figure 4b, Z' and Z'' can be expressed as

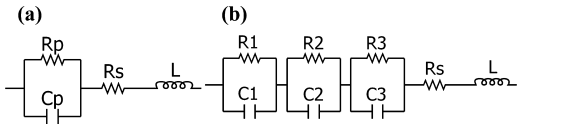

Figure 4. (a) Typical equivalent circuit model of a Schottky diode. C_P denotes the depletion layer capacitance of the contact, R_P is associated with a shunt resistance, and R_S is a series resistance. (b) Extended equivalent circuit model with C_1, C_2, and C_3 being capacitances with corresponding shunt resistances R_1, R_2, and R_3, associated with a nickel−carbon interface, a carbon−silicon interface, and a silicon-titanium interface, respectively. R_S is the series resistance, and L represents a parasitic inductance associated with the electrical leads.

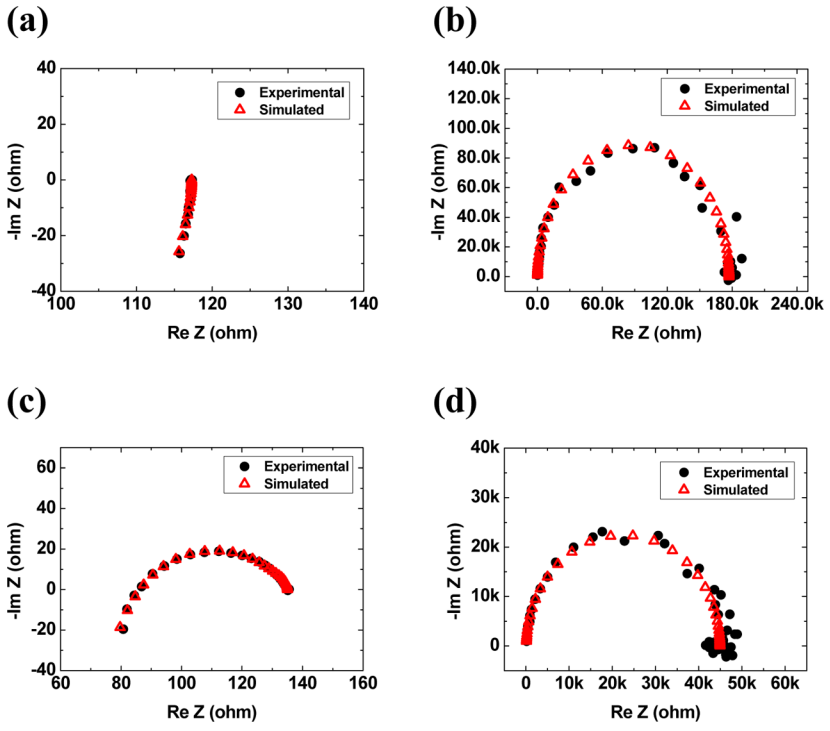

Figure 5. Cole−Cole plots and corresponding fit from the equivalent circuit model of Figure 4b on the PPF/n-Si SBD under dc bias of (a) +0.4 V and (b) −0.4 V, and the PyC/n-Si SBD under dc bias of (c) +0.4 V and (d) −0.4 V.

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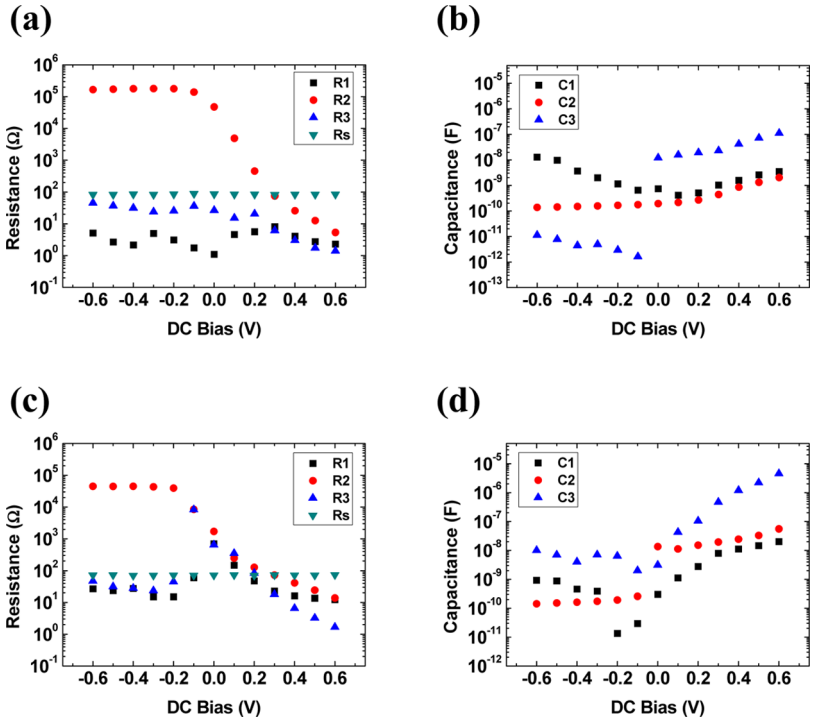

Figure 6. Resistance and capacitance values for dc bias voltages in the range of +0.6 to −0.6 V obtained from the best fit of the measured impedance spectra of the PPF/n-Si (a, b) and PyC/n-Si (c, d) SBDs using the equivalent circuit model of Figure 4b.

$$Z'(\omega) = \frac{R_1}{1 + (\omega R_1 C_1)^2} + \frac{R_2}{1 + (\omega R_2 C_2)^2} + \frac{R_3}{1 + (\omega R_3 C_3)^2} + R_S \quad (9)$$

$$Z''(\omega) = \frac{\omega R_1^2 C_1}{1 + (\omega R_1 C_1)^2} + \frac{\omega R_2^2 C_2}{1 + (\omega R_2 C_2)^2} + \frac{\omega R_3^2 C_3}{1 + (\omega R_3 C_3)^2} - \omega L \quad (10)$$

The fitted curves for forward (+0.4 V) and reverse (−0.4 V) bias data based on these equations are shown in Figure 5, which clearly presents a good fit between the experimental and simulated data. It was also verified that the simulated data from the equivalent model of Figure 4b led to a similarly good fit with the experimental data under various dc biases (see Supporting Information Figures S2 and S3). The values of resistance and capacitance obtained from the best fit of the measured impedance are plotted in Figure 6 for both carbon−silicon SBD devices, and detailed data are presented in the Supporting Information (Tables S1and S2). The R_S of each device has a constant average value of 85 Ω for the PPF/n-Si SBD and 72 Ω for the PyC/n-Si SBD device. These do not show any significant change under different dc bias voltages and are in agreement with the R_S values from the dc $J-V$ measurements. On the contrary, R_2 undergoes dramatic change when the dc bias is changed from the reverse region to the forward region in both devices. Moreover, R_2 has very high resistance values compared to R_1 and R_3 in the reverse dc bias regime, which clearly indicates that the R_2C_2 component is associated with the Schottky barrier between carbon and silicon because R_2 blocks the current flow through the junction under reverse dc bias. In the forward dc bias regime, R_2 drops significantly as the bias voltage increases, which makes sense given that more carriers are injected into the Schottky junction and thus the junction resistance drops when the forward dc bias voltage is raised. The other RC network components (R_1C_1 and R_3C_3) of the circuit, associated with the nickel−carbon interface and silicon−titanium interface, respectively, show only small variations under different dc bias conditions. In the ideal case, each metal electrode contact should have a constant value for its resistance and capacitance; however, possible defects on the surface of carbon thin films and the backside of silicon substrates can cause such variation. In addition, possible contributions from the edges of the diode structures such as fringe capacitances or changed interfaces due to the oxygen plasma etching or direct contact with air could result in bias dependent behavior of the interface.These local resistance components can be distinguished using ac impedance analysis, something which is impossible with dc analysis where all of the resistance components merely contribute to a single series resistance.

Using the capacitance values (C_2) corresponding to the Schottky contact of the devices derived from the impedance spectra, plots of $1/C^2$ against the reverse dc bias voltage can be obtained for each carbon−silicon SBD device, giving information on the built-in potential and the barrier height of the Schottky contact.[2] In general, capacitance measurements are widely used for determining the built-in potential in M-S contactsby analysis of the capacitance−voltage ($C-V$) characteristics. However, it has been revealed that the presence of series resistances in structures with potential barriers can have a significant effect on the measured capacitance with conventional capacitance measurements. Thus, differing from the true barrier capacitance, an ac analysis method based on IS is proposed to prevent errors arising from series resistances.[25] According to the $C-V$ relationship at the depletion layer of a metal−semiconductor M-S contact, $1/C^2$ and V have a linear

relationship and the intercept value (V_i) of the x-axis can be found from plots based on the following equations[2]

$$\frac{1}{C^2} = \left(\frac{2}{\varepsilon_S q N_d}\right)(V_i - V) \tag{11}$$

$$V_i = V_{bi} - (k_B T/q) \tag{12}$$

where ε_S is the permittivity of the silicon substrate, N_d is the silicon dopant concentration, and V_{bi} is the built-in potential of the Schottky contact. $1/C^2$ vs V plots for the devices are shown in Figure 7, and they give built-in potential values of 0.62 V for

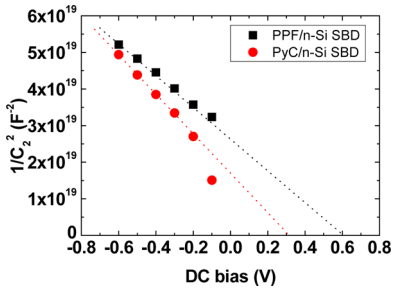

Figure 7. Plot of $1/C^2$ vs V for the PPF/n-Si and PyC/n-Si SBDs with C_2 values derived from the simulated results using the equivalent circuit model of Figure 4b.

the PPF/n-Si SBD and 0.32 V for the PyC/n-Si SBD. In addition, the value of the Schottky barrier height can be calculated using the equation below[2]

$$\phi_B = V_{bi} + \frac{(E_C - E_F)}{q} = V_{bi} + \left(\frac{k_B T}{q}\right)\left[\ln\left(\frac{N_c}{N_d}\right)\right] \tag{13}$$

where E_C is the energy of the conduction band edge, E_F is the energy of the Fermi level, and N_c is the effective density of states in the conduction band of n-type silicon. The determined barrier heights from eq 13 are 0.91 eV for the PPF/n-Si SBD and 0.61 eV for the PyC/n-Si SBD. When comparing the values of the Schottky barrier height from the $C-V$ characteristics to the values from the $J-V$ results (which are 0.78 eV for the PPF/n-Si SBD and 0.49 eV for the PyC/n-Si SBD), there is a slight discrepancy with a shift of 0.12−0.13 eV to higher values in both cases, which means that the PPF/n-Si SBD has a barrier 0.3 eV higher than the PyC/n-Si SBD. The discrepancy may stem from the presence of an insulating layer or charges exiting at the carbon−silicon interface;[26] however, this is not clearly visible in the cross-sectional TEM images. A thin oxide or insulating layer can form at the junction of Schottky diodes unless all the processing is done in high vacuum.[26] In our case, this is more likely to occur for the PyC SBD, as the carbon deposition takes place in a high temperature environment, as opposed to the PPF, which is spun on at room temperature prior the high temperature anneal, protecting the interface from oxidation. Furthermore, using the thermionic emission model to calculate the barrier height neglects contributions from deep levels which possibly occur in the silicon band gap and image force lowering, meaning the $J-V$ results yield an underestimated barrier height. The present method reveals that detailed analysis of the electrical characteristics can result in an understanding of the electrical properties of various carbon nanostructures and this could be extended to further material sets and their interfaces.

4. CONCLUSION

In summary, the electrical properties of carbon−silicon Schottky contacts in high performance SBD devices have been explored using both dc $J-V$ measurements and ac impedance measurements. Two different conductive carbon thin films, PPF and PyC, were employed to create the Schottky contacts on n-type silicon substrates. Diode parameters including the ideality factor, the Schottky barrier height, and the series resistance were extracted on the basis of thermionic emission theory from dc $J-V$ measurements. In addition, a more detailed investigation of the Schottky contact with IS analysis under various dc biases has been carried out. An equivalent circuit model of the SBD taking into account second-order effects such as capacitance from the metal electrode contacts and parasitic inductance has been proposed to identify the built-in potential and the barrier height values at the Schottky junction. The electrical characteristics of the Schottky contact between the carbon thin films and the silicon substrates were verified using RC values extracted from the equivalent circuit model. Thus, IS can be utilized for the evaluation and the simulation of Schottky contacts and allows for a better understanding of interfaces on a fundamental level.

■ ASSOCIATED CONTENT

Supporting Information

Additional details on ac impedance spectra analysis with equivalent circuit models. Figure S1: Cole−Cole plots and corresponding best fits from the equivalent circuit models of Figure 4 on each carbon−silicon SBD. Figures S2 and S3: additional Cole−Cole plots and corresponding best fits of each carbon−silicon SBD device from the equivalent circuit model of Figure 4b under various dc biases. Tables S1 and Table S2 summarizing the values of resistance, capacitance, and inductance (R_1, C_1, R_2, C_2, R_3, C_3, R_S, L) along with the applied dc bias voltages from +0.6 to −0.6 V obtained from the best fit of the measured impedance spectra of the carbon−silicon SBDs using the equivalent circuit model of Figure 4b. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Author

*E-mail: duesberg@tcd.ie. Tel.: +353-1-896-3035.

Author Contributions

C.Y. and G.S.D. conceived and designed the experiments. N.M. synthesized the PyC thin film, and E.R. performed HRTEM analysis. C.Y. performed the experiments. C.Y., H.-Y.K., and G.S.D. analyzed the data. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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